Electronic Version
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Claims

[c1] What is claimed is:

1. A method for fabricating a semiconductor device comprising:

providing a substrate, at least one first gate structure and at least one second gate structure being included on a surface of the substrate, both the first gate structure and the second gate structure having sidewalls;

performing a first ion implantation process to form a shallow-junction doping region of a first conductive type in the substrate next to each of the sidewalls of the first gate structure;

forming offset spaces on each of the sidewalls of the first gate structure and the second gate structure; and

performing a second ion implantation process to form a shallow-junction doping region of a second conductive type in the substrate next to the offset spacer on each of the sidewalls of the second gate structure.

[c2] 2. The method of claim 1 wherein the substrate comprises a silicon substrate or a silicon-on-insulator substrate.

[c3] 3. The method of claim 1 wherein both the first gate

structure and the second gate structure comprise a polysilicon gate and a gate dielectric layer interposed between the polysilicon gate and the substrate.

[c4] 4. The method of claim 1 wherein a dopant of the first implantation process comprises phosphorous or arsenic, and the first gate structure is a gate of an input/output (I/O) NMOS.

[c5] 5. The method of claim 1 wherein the method for forming the offset spacer on each of the sidewalls of the first gate structure and the second gate structure further comprises the following steps:
forming a dielectric layer on the surface of the substrate to cover the first gate structure and the second gate structure; and
performing a dry etching process to vertically remove the dielectric layer down to the surface of the substrate.

[c6] 6. The method of claim 5 wherein the dielectric layer is a tetra-ethyl-ortho-silicate (TEOS) oxide layer formed by a low temperature chemical vapor deposition (LPCVD) process at a temperature ranging from 650°C to 680°C.

[c7] 7. The method of claim 6 wherein a thickness of the TEOS oxide layer ranges from 170 to 210 angstroms (Å).

[c8] 8. The method of claim 1 wherein a dopant of the sec-

ond ion implantation process is boron, and the second gate structure is a gate of an input/output (I/O) PMOS.

[c9] 9. The method of claim 1 wherein at least one third gate structure is included on the surface of the substrate, an offset spacer is simultaneously formed on each sidewall of the third gate structure when forming the offset spacers on each of the sidewalls of the first gate structure and the second gate structure.

[c10] 10. The method of claim 9 further comprising the following steps after performing the second ion implantation process:
forming a spacer layer on the surface of the substrate to cover the first gate structure, the second gate structure, the third gate structure, and the offset spacers on each of the sidewalls of the first gate structure, the second gate structure, and the third gate structure; and
performing an etching process to form a spacer at sides of the first gate structure, the second gate structure, and the third gate structure.

[c11] 11. The method of claim 9 further comprising at least one third ion implantation process after performing the second ion implantation process to form a lightly doped drain region in the substrate next to the offset spacer on each of the sidewalls of the third gate structure.

[c12] 12. The method of claim 9 further comprising at least one pocket ion implantation process after performing the second ion implantation process to form a pocket doping region in the substrate at either side of the first gate structure, the second gate structure, and the third gate structure.

[c13] 13. The method of claim 10 further comprising at least one fourth ion implantation process after performing the etching process to form a source/drain region in the substrate next to the spacer at either side of the first gate structure, the second gate structure, and the third gate structure.

[c14] 14. The method of claim 1 wherein the step for forming the offset spacers on each of the sidewalls of the first gate structure and the second gate structure is used for improving the hot carrier immunity ability of the semiconductor device.

[c15] 15. A method for fabricating a semiconductor device comprising:
providing a substrate, at least one gate structure of a PMOS and at least one gate structure of an NMOS being included on a surface of the substrate, both the gate structure of the PMOS and the gate structure of the

NMOS having sidewalls;

performing an N-type ion implantation process to form an N-type source/drain (S/D) extension in the substrate next to each of the sidewalls of the gate structure of the NMOS;

forming offset spacers on each of the sidewalls of the gate structure of the NMOS and the gate structure of the PMOS; and

performing a P-type ion implantation process to form a P-type S/D extension in the substrate next to the offset spacer on each of the sidewalls of the gate structure of the PMOS.

[c16] 16. The method of claim 15 wherein the substrate comprises a silicon substrate or a silicon-on-insulator substrate.

[c17] 17. The method of claim 15 wherein both the gate structure of the PMOS and the gate structure of the NMOS comprise a polysilicon gate and a gate dielectric layer interposed between the polysilicon gate and the substrate.

[c18] 18. The method of claim 15 wherein a dopant of the N-type ion implantation process comprises phosphorous or arsenic, and a dopant of the P-type ion implantation process is boron.

[c19] 19. The method of claim 15 wherein the method for forming the offset spacer on each of the sidewalls of the gate structure of the NMOS and the gate structure of the PMOS further comprises the following steps:
forming a dielectric layer on the surface of the substrate to cover the gate structure of the NMOS and the gate structure of the PMOS; and
performing a dry etching process to vertically remove the dielectric layer down to the surface of the substrate.

[c20] 20. The method of claim 19 wherein the dielectric layer is a tetra-ethyl-ortho-silicate (TEOS) oxide layer formed by a low temperature chemical vapor deposition (LPCVD) process at a temperature ranging from 650°C to 680°C.

[c21] 21. The method of claim 20 wherein a thickness of the TEOS oxide layer ranges from 170 to 210 angstroms (Å).

[c22] 22. The method of claim 15 where the NMOS is an input/output (I/O) NMOS, and the PMOS is an I/O PMOS.

[c23] 23. The method of claim 15 wherein at least one gate structure is included on the surface of the substrate, an offset spacer is simultaneously formed on each sidewall of the gate structure when forming the offset spacers on each of the sidewalls of the gate structure of the NMOS and the gate structure of the PMOS.

[c24] 24. The method of claim 23 further comprising the following steps after performing the P-type ion implantation process:
forming a spacer layer on the surface of the substrate to cover the gate structure of the PMOS, the gate structure of the NMOS, the gate structure, and the offset spacers on each of the sidewalls of the gate structure of the PMOS, the gate structure of the NMOS, and the gate structure; and
performing an etching process to form a spacer at sides of the gate structure of the PMOS, the gate structure of the NMOS, and the gate structure.

[c25] 25. The method of claim 23 further comprising at least one first ion implantation process after performing the P-type ion implantation process to form a lightly doped drain region in the substrate next to the offset spacer on each of the sidewalls of the gate structure.

[c26] 26. The method of claim 23 further comprising at least one pocket ion implantation process after performing the P-type ion implantation process to form a pocket doping region in the substrate at either side of the gate structure of the PMOS, the gate structure of the NMOS, and the gate structure.

[c27] 27. The method of claim 24 further comprising at least one second ion implantation process after performing the etching process to form a source/drain region in the substrate next to the spacer at either side of the gate structure of the PMOS, the gate structure of the NMOS, and the gate structure.

[c28] 28. The method of claim 15 wherein the step for forming the offset spacers on each of the sidewalls of the gate structure of the NMOS and the gate structure of the PMOS is used for improving the hot carrier immunity ability of the semiconductor device.